REMARKS/ARGUMENTS:

Claims 40, 41, 47, 60, 61, 63-74, 76-79 and 81-84 are now pending in the application for consideration. Claims 40, 62 and 79 have been amended. No new claims have been added.

The amendments made to claims 40, 62 and 79 are solely by way of clarification and are not intended to limit the claims with respect to the prior art. Rather, the change in each of claims 40, 62 and 79 is made for clarification in view of the teaching of applicants' specification at page 13, lines 1-3 that annealing is "preferably at a temperature of at least about 200^{o}C up to the melting point or decomposition temperature of other components of the device, . . ." and is consistent with a corresponding recitation in claim 80.

Claim Rejections under 35 US 103

In the Office Action mailed September 29, 2003, all pending claims were rejected under 35 US 103, the independent claims being rejected as follows:

Claim 81 as unpatentable over WO 94/19829 (Lisenker) in view of US Patent 5,434,440 (Yoshitomi).

Claim 40 as unpatentable over any one of US Patents 4,027,380 (Deal), 4,212,100 (Paivinen), 5,198,880 (Taguchi), and 5,320,975 (Cederbaum) in view of Lisenker.

Claims 62, 76, 79, 80 and 81 as unpatentable over any one of Deal, Paivinen, Taguchi, or Cederbaum in view of Lisenker and further in view of US Patent 5,434,440 (Yoshitomi).

Lisenker.

Initially, it is noted that Lisenker presents a solely academic, theoretical disclosure unverified by any practical experimental results. Applicant's maintain the interpretation of Lisenker as discussed in previous responses, in particular in the response dated May 13, 2003. Applicants' interpretation of Lisenker is supported by the Wallace Declaration, see Sections 11-14, as discussed in more detail herein with reference to rejection of particular claims.

Lisenker's theoretical teaching, as developed at page 7, lines 30 – 36 of Lisenker, is evaluated

in Section 11 of the Wallace Declaration to "indicate that the Si-D (or Si-OD) bond is slightly less susceptible to bond scission upon thermal activation than the analogous Si-H (Si-OH) bond." Lisenker also teaches ". . . the kinetic isotope effect in the chemical reactions requires that deuterium containing bonds break more slowly than the corresponding hydrogen containing bonds" – i.e. a reduction in the rate of Si-D bond scission relative to that observed for Si-H bond scission – and Lisenker indicates an improvement factor of roughly 2-3. (Lisenker, page 8, lines 3-12.) Such a small change would have been within the normal range of process parameter variations using hydrogen or forming gas annealing. Based on the solely theoretical teaching of Lisenker, which as noted by the Examiner, *". . . is not a post metal anneal . . .",* and the small predicted kinetic isotope effect, one of ordinary skill in the art would not have been motivated to explore employment of deuterium in place of hydrogen in the well established post metal hydrogen annealing process widely in use in the semiconductor industry at the time of the invention claimed in the present application. (Wallace Declaration, section 11.)

In rejecting claims 81 and 82, the Examiner is dismissive of the claim element ". . . deuterium introduced into and remaining within said [gate insulator] film": *"Claim 81 . . . merely requires a concentration of deuterium remaining in the film."* This characterization by the Examiner completely ignores the practical importance of the claim limitation. Claim 81 further defines ". . . said concentration of deuterium substantially reducing said degradation associated with said hot carrier stress." In device operation(see applicants' specification, e.g. page 17, lines 13-21), it is the retained deuterium in the device that functions to provide the efficacious improvement in device resilience to hot carrier effects resulting from electrical stress. Applicants demonstrated at least an order of magnitude improvement in device lifetime as compared with identical devices subjected to post metal hydrogen annealing under identical annealing conditions. (Applicants specification page 17, line 1 to page 18, line 10.) Manifestly, the "remaining within said film" limitation in claim 81 and also the ""retention of deuterium" limitation in claim 40 are not lightly to be dismissed but must be given weight in contributing to the patentability and non-obviousness of those claims, each considered as a whole. See MPEP 2143.03.

No hint at the dramatic reductions in device degradation associated with hot carrier stress made possible by the claimed invention would have been provided to a person of ordinary skill in the art by Lisenker's disclosure. Lisenker suggested, at most, a very modest 2-3 factor improvement in kinetic isotope effect by employment of deuterium instead of hydrogen in Lisenker's disclosed process, the shortcomings of which have been addressed above. Not only would such a small improvement (as compared with conventional hydrogen annealing) not have motivated a person of ordinary skill in the art to have employed Lisenker's teaching, but, as studies subsequent to the filing date of the present application have shown, deuterium introduced by pre-metal annealing is prone to dissipation during subsequent thermal treatments. (Wallace Declaration Sections 13, 14, Exhibits A, B, C cited therein, and W.F. Clark et al., *"Process Stability of Deuterium-Annealed MOSFET's"*, IEEE Electron Device Letters, Vol. 20, No. 1, pages 48-50, January 1999, Wallace Exhibit G.)

While the presence of deuterium remaining in the gate insulator film is obtained from post-fabrication annealing disclosed in the present application, applicant is entitled to claim, as in claim 81, the resulting structure, including the structural feature "a concentration of deuterium introduced into and remaining within said film, . . . said concentration of deuterium substantially reducing said degradation associated with said hot carrier stress" without recitation of the process parameters used. As discussed above, and addressed in subsequent discussion, deuterium introduced by pre-metal processing, as disclosed by Lisenker, would be dissipated by subsequent thermal treatments and consequently the resultant device would not include a *remaining* "concentration of deuterium substantially reducing said degradation associated with said hot carrier stress", as required by claim 81. Likewise, the feature reciting "retention of deuterium" recited in claim 40 is not anticipated by nor would it have been rendered obvious by Lisenker.

Thus, regardless of Yoshitomi, cited only for teaching "growing a gate oxide . . . having a thickness of 4nm (40 angstroms)", claims 81 and 82 would not have resulted from, or have been rendered "obvious" under 35 US 103 by, Lisenker's teaching.

In rejecting independent claims 40, 62, 76, 79, 80 and 81, the Examiner uses Deal,

Paivinen, Taguchi, or Cederbaum as a primary reference and Lisenker as a secondary reference. The primary references show employment of hydrogen (or a hydrogen and nitrogen mixture) annealing for different purposes, in processing MOS devices. In particular, Deal discloses a post-metal annealing of a CMOS structure "to minimize the fast interface state density" (col. 9, lines 33-51). Paivinen discloses that an "aluminum blanket [that has been deposited over top surface of the structure] is presintered for about 5 minutes at about 400°C in forming gas (10% hydrogen and 90% nitrogen) to provide improved metallurgical bonding between the metal blanket and the polysilicon portions remaining on the substrate 22." (Col. 6, lines 5-10.) Taguchi's incidental disclosure relating to forming gas processing of a structure utilizing a "gate oxide film having a thickness of 700A" after forming "aluminum wiring films", relied on by the Examiner, is: "Finally, a forming gas treatment is performed for the substrate at a temperature of 450°C. (FIG. 1)" Cederbaum teaches that "to increase the channel mobility and decrease the threshold voltage VT of the pFETs, hydrogen passivation of the dangling bonds is required", stating "this step known in the art as the 'forming gas anneal step' is completed in a furnace at 400°C. During 30 mn, in a N_2/H_2 forming gas" and that the step "can be repeated several times during the BEOL [Back End Of Line] process." (Col 13, line 62 to col. 14, line 24.) Thus, all of these references address the use of forming gas annealing for disparate purposes not pertinent to the structure claimed in any of claims 40, 62, 76, 79, 80 and 81 and their dependent claims.

None of these references appears to be concerned with reducing deleterious hot carrier effects on device operation. None of these references is seen to have suggested or to have provided motivation to a person of ordinary skill in the art to have modified their annealing processes by employment of Lisenker's pre-metal anneal teaching. And, neither is Lisenker seen to provide motivation -- Wallace Declaration, Section 11. Nor, in contrast to the presently claimed invention, is Deal, Paivinen, Taguchi, or Cederbaum seen to be concerned with providing a semiconductor device having improved operational characteristics in terms of increased resilience to hot carrier effects resulting from electrical stress, and consequently their teachings are not germane to the device structure claimed in the present application. It is again emphasized that at the time of the present invention, post metal hydrogen (or hydrogen/nitrogen mixture) had been long established and widely employed in post metal annealing processes in semiconductor process technology (Exhibit H to Wallace Declaration)

and it has been demonstrated by the above discussion that Lisenker provided no motivation for change – Wallace Declaration Section 11.

In rejecting claim 40, the Examiner asserts:

> "Neither criticality nor unexpected results are shown for post annealing in deuterium (claimed invention) relative to annealing in deuterium before contacts are formed. The data in the specification, including Figs. 2-3, compares annealing in deuterium relative to annealing in hydrogen. Annealing in hydrogen is not the closest prior art. The closest arior art reference is Lisenker. Applicants have not shown that annealing post-metallization in deuterium is critical or has unexpected results relative to pre-metal annealing in deuterium (i.e., Lisenker).

This assertion is rebutted by the Wallace Declaration, Section 12 describes motivation by himself and his coworkers to" examine the improvements in device reliability reported by Lyding et al., the results of their study, consistent with the results obtained by Lyding *et al* in the "EXPERIMENTAL" disclosed in the present application, - see Wallace Declaration, Exhibit A. The Wallace Declaration, Section 15, also traverses the Examiner's contention that Lisenker, rather than post-metal hydrogen annealing is the closest prior art.

In rejecting independent claims 62, 76, 79, 80, 81 and their dependent claims 63, 77, 78, 82 and 84, the Examiner frames the issue as " whether it would have been obvious to one of ordinary skill in the art at the time of applicant's invention . . . to modify the post metal deuterium anneal that is suggested in the prior art by applying it to a transistor having a gate oxide thickness of less than 55 angstroms." However, the Examiner has signally failed to demonstrate substantial evidence of any such suggestion in the prior art exemplified by Lisenker, Yoshitomi, Deal, Paivinen, Taguchi, or Cederbaum, or by then accepted practices in the art. The Examiner's assertion is strenuously traversed based on the foregoing discussion as well as on the basis of the Wallace Declaration, noting in particular Section 12. That gate oxide thickness of less than 55 angstroms was known at that time is not determinative of obviousness of a combination of elements as set forth in any of claims 62, 63, 76-82 and 84. The issue is whether the prior art would have suggested the combination of elements as recited in any of those claims, each considered as a whole, and the Examiner has not established a prima facie case of obviousness within those parameters. Rather, the Examiner has attempted to put

together a hypothetical mosaic of features carefully extracted from prior art documents, using applicants' claimed invention as a roadmap. This is not only impermissible hindsight reconstruction of the claimed invention but also falls short of meeting the combination of elements as recited in each of claims 62, 63, 76-82 and 84 under rejection as has been discussed above, and shown in the Wallace Declaration, Sections 11, 13 and 14.

With respect, the Examiner's attention is drawn to comments by the CAFC in *In re Kotzab* 55 USPQ2d 1313 (CA FC 2000), quoted in pertinent part:

> A critical step in analyzing the patentability of claims pursuant to section 103(a) is casting the mind back to the time of invention, to consider the thinking of one of ordinary skill in the art, guided only by the prior art references and the then-accepted wisdom in the field. See Dembiczak, 50 USPQ2D at 1617. Close adherence to this methodology is especially important in cases where the very ease with which the invention can be understood may prompt one "to fall victim to the insidious effect of a hindsight syndrome wherein that which only the invention taught is used against its teacher." Id. (quoting W.L. Gore & Assocs., Inc. v. Garlock, Inc., 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983)).
>
> Most if not all inventions arise from a combination of old elements. See In re Rouffet, 47 USPQ2D 1453, 1457 (Fed. Cir. 1998). Thus, every element of a claimed invention may often be found in the prior art. However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant. See In re Dance, 48 USPQ2D 1635, 1637 (Fed. Cir. 1998); In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984).

Note also MPEP 2143.01, particularly under the headings "FACT THAT REFERENCES CAN BE COMBINED OR MODIFIED IS NOT SUFFICIENT TO ESTABLISH *PRIMA FACIE* OBVIOUSNESS" and "FACT THAT THE CLAIMED INVENTION IS WITHIN THE CAPABILITIES OF ONE OF ORDINARY SKILL IN THE ART IS NOT SUFFICIENT TO ESTABLISH *PRIMA FACIE* OBVIOUSNESS".

The analysis of the prior art in rejecting claims 62, 63, 76-82 and 84 arbitrarily selects individual features of those claims and then attempts to correlate them to the cited prior art references, glossing over contextual limitations of the references and inadequately considering the content of each claim considered as a whole. It is error to attempt such reconstruction using applicant's claim as a blueprint; *W.L. Gore & Associates, Inc. v. Garlock, Inc., 220 USPQ 303 (CAFC 1985).* The mere fact that the prior art could be modified to form the invention as defined in these claims does not make the modification obvious absent suggestion by the prior

art of the desirability of the modification to obtain the claimed combination of elements as recited in the claims; *In re Laskowski, 10 USPQ2d 1297 (CAFC 1989).* As discussed above, none of Deal, Paivinen, Taguchi or Cederbaum is concerned with producing a semiconductor device that ameliorates the degrading effects on operating characteristics of electrical stress induced hot carriers. Applicants discovered that, post metal deuterium annealing could enable production of a semiconductor device (in particular an insulated gate field effect transistor device) having efficacious operating characteristics in terms of a significant (by at least an order of magnitude) increase in device lifetime, particularly significant in semiconductor devices employing a "thin" gate insulator, as compared with an identical device subjected hydrogen annealing using the same annealing parameters (see applicants' specification pages 14 to page 17, line 21). The substantial benefits were demonstrated by practical experimentation (rather than a theoretical proposal) showing device improvement in terms of device lifetime by an order of magnitude (see applicants' specification, page 17, line 22 to page 18, line 10). Claims 62, 63, 76-82 and 84 recite combinations of features consistent with applicants' discovery and none of those claimed inventions, considered as a whole, would have been suggested by the prior art at the time of applicants' invention.

For completeness, it is noted that the Examiner's assertion, in rejecting claims 76-78: "It would have been obvious . . . to select an anneal duration of one hour at 450°C using a 10% hydrogen 90% nitrogen composition as claimed . . ." is incorrect and it is presumed the assertion contains a typographical error. The rejection of claims 76-78 has been traversed as discussed above.

Examiner's Response to Arguments

The substance of the Examiner's response has been addressed either in the above discussion or in the Declaration under 37 CFR 132. However, there are two points that require specific comment.

First, the Examiner states:

> Additionally, applicants state in their specification that benefits can be achieved by introducing deuterium at stages other than post fabrication. There came a time when applicant suggested on this record (response to office action #2, filed 08-02-99, page 4) that these resulted should be considered in the obviousness inquiry as part of the invention as a whole."

With respect, this is a mischaracterization of the content of that response (perhaps due to reliance of a single paragraph taken out of context – *vide* earlier comments concerning interpretation of cited references by the Examiner. The paragraph cited by the Examiner clearly is directed to and qualified by the content of the paragraph that precedes it in the response:

> "Neither WO 94/19829 nor Saks et al. teaches that passivation should be conducted post-fabrication, . . . sufficiently to achieve high-level increases in transistor lifetime, as claimed." Emphasis added.

Withdrawal of the Examiner's assertion would be appreciated.

Second, the Examiner asserts:

> Those who have recognized post-metallization annealing with deuterium, U.S. Pat. No. 6,328,801 ("Gary"), attribute the invention to Lisenker."

Using the USPTO website patent search facility, under Advanced Search, with a search parameter "FREF/WO94/19829", located a single patent, namely, US Pat. 6,328,801. With respect, the Examiner's assertion does appear to be somewhat exaggerated. A more balanced and objective assessment is apparent from the following publications:

W.F. Clark, et al. in "Improved Hot-Electron Reliability in High-Performance, Multilevel-Metal CMOS Using Deuterated Barrier-Nitride Processing", *IEEE Electron Device Letters*, vol. 20, No. 10, pp. 501-503, October 1999 – see p.501, Introduction, lines 1-14. (Copy provided for the Examiners convenience.) There, Clark et al. provide the following characterizations:

> "Several years ago, the use of deuterium was proposed to reduce NMOS-transistor susceptibility to hot-carrier degradation by hardening the silicon/silicon dioxide interface." – citing Lisenker WO94/19829

followed by:

> "Recent studies have shown that the replacement of standard hydrogen-based post-metal anneals with deuterium-ambient anneals have yielded significant improvements in hot-electron lifetimes."

-citing a Lyding et al. paper "Reduction of hot-electron degradation in metal-oxide semiconductor transistors by deuterium processing," *Appl. Phys. Lett.*, vol. 68, no. 18, p.2526, 1996 (Wallace Declaration - Exhibit F) The annealing processing described in that paper corresponds to that described in the specification of the present application, pages 18 - 23.

Note the distinction in characterization of Lisenker as a proposal versus the recognition of the post-metal annealing of Lyding et al. as having "yielded significant improvements", i.e. a practical implementation.

Note also J. S. Murday, "Nanoscience Fostering Technology", IUVTA Highlight Seminar (2 pages – downloaded from www.iuvsta.org/nanohighlights.html) believed (on the basis of reasonable inquiry) to have been presented at *5th International Conference on Nanometer Science and Technology (NANO-5)*, Birmingham, UK, 31 August - 4 September 1998:

> "Lyding and Hess (2) have contributed another technologically important piece of science involving H and silicon. Lyding, among several others, has demonstrated that a proximal probe can be desorb H from a H compensated Si (100) surface with near atomic precision. While investigating the desorption mechanism, he noted D desorption was far more retarded than expected from simple models of mass effects. Hess and Lyding realized that this observation could have dramatic impact on MOS devices. Hydrogen is presently diffused into the Si / SiO interface of MOS structures to tie off trap states which degrade the device performance characteristics. A principle failure mechanism for the devices has been electron induced disruption of those Si-H bonds. The substitution of D for H has been shown to dramatically improve the lifetime of those devices. This improvement in reliability allows the device designer to reduce the device dimensions; the result will be more rapid progress toward higher clock frequencies."

Thus, there has been independent peer recognition by others in the art that significant (unexpected) results have been obtained by post-metal annealing, as claimed in the present application, relative to the closest art actually practiced in the industry, (rather than relative to an academic, paper proposal) and these benefits have been attributed to post-metal annealing "rather than annealing at any other stage in the process", to use the Examiner's

characterization. Note also the Wallace Declaration, Sections 12 and 15. Accordingly, there has been substantial evidence of recognition in the art of the contributions made by the invention made by Lyding and Hess as claimed in claims pending in this application and hence of the non-obviousness of that invention.

Conclusion.

In summary, the Examiner has failed to establish a prima facie case of obviousness meeting the criteria contained in MPEP 2142 and 2143, while applicants have established that the cited prior art fails to teach or suggest the claimed invention and have demonstrated evidence of significant improvement over the closest practical art and independent recognition of the claimed invention in the art.

Entry of this amendment and early allowance of all pending claims will be appreciated. If discussion would assist in moving forward prosecution of this application, a telephone call to the undersigned attorney (972-826-7428) would be appreciated.

Date: March 26 2004

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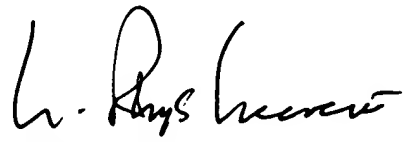
Respectfully submitted,



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IUVSTA Highlight Seminar

Nanoscience Fostering Nanotechnology

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The 1991 Binnig, Rohrer et. al. Physical Review Letter on STM imaging of silicon kicked-started the present era with emphasis on the science and technology of nanometer structures. Sixteen years later, the science base has expanded dramatically. Our ability to analyze and fabricate nanometer sized structures has expanded in scope and sophistication.

We are now approaching the time frame associated with the development of new products from science innovation. Does the frequently used word nanotechnology mean very small amounts of technology, or is there evidence for imminent technology based on nanometer structures?

In my opinion, the science of nanometer structures will have the most dramatic impact in three areas: electronics / optoelectronics; molecular biology, biotechnology and medicine; and materials affordability. Let me show evidence for imminent technology for the first two by citing examples taken largely from the Naval Research Laboratory and the Office of Naval Research..

Electronic / optoelectronic devices have depended on nanometer dimensions for over a decade - thin films and superlattice structures require dimensional tolerance perpendicular to the interface at the nanometer and, increasingly, atomic level. One straightforward, but important, technology contribution has come from the proximal probes which enabled the visualization of surface topographies. Near real time imaging can lead to spectacular improvements in the nucleation/growth of semiconductor surfaces; at NRL we have demonstrated this for the growth of InAs on GaAs. But the power of STM/S goes beyond establishing topology. In a combined experimental and theoretical tour de force, Whitman et al (1) have established guidelines for understanding the vicinal surface structures on silicon crystals. The surface reconstructions are influenced by a delicate balance between the energies associated with dangling bonds and with strained bond angles/separations. The pristine surface reconstructions for planes between Si (001) and Si (111) are now reasonably well understood, and work-to-date on the effects of hydrogen chemisorption on those reconstructions shows no surprises. There are significant technology ramifications to this science because heteroepitaxy plays an important part in evolving electronic devices; the effect of substrate structure on the growth process is crucial.

Lyding and Hess (2) have contributed another technologically important piece of science involving H and silicon. Lyding, among several others, has demonstrated that a proximal probe can be desorb H from a H compensated Si (100) surface with near atomic precision. While investigating the desorption mechanism, he noted D desorption was far more retarded than expected from simple models of mass effects. Hess and Lyding

realized that this observation could have dramatic impact on MOS devices. Hydrogen is presently diffused into the Si / SiO interface of MOS structures to tie off trap states which degrade the device performance characteristics. A principle failure mechanism for the devices has been electron induced disruption of those Si-H bonds. The substitution of D for H has been shown to dramatically improve the lifetime of those devices. This improvement in reliability allows the device designer to reduce the device dimensions; the result will be more rapid progress toward higher clock frequencies.

Three dimensional nanostructured electronics is still largely a dream. However, if continued miniaturization of electronic devices is to continue beyond the year 2015, this dream must be converted into a reality. Proximal probes have demonstrated the ability to fabricate structures atom-by-atom. The timeframe for a entire 10 cm semiconductor wafer surface fabrication, atom-by-atom, would be centuries - a bit long for most commercial markets. A single proximal probe suffers from this constraint of serial processing. However, proximal probes can be microfabricated and Quate (3) has now constructed 50 individually addressable proximal probes on a single Si wafer. In a demonstration for the NANO IV conference in China, his group wrote out that word using two separate tips for the first and last three letters.

Membrane functionality, the molecular recognition basis of immunoresponse, DNA and protein structure - all involve nanometer structures. It is on this basis I contend that biotechnology and medicine will be dramatically impacted by nanoscience. A particularly illustrative example is found in the work of Lee (4) who has used proximal probes to measure the forces associated with disruption of single molecule antibody/antigen bonds and pairing between complementary DNA strands. While this work has provided key insights which complement the traditional thermodynamic approaches to macromolecular folding , it also has stimulated what might become a revolution in immunoassay technology (5). Immunoassays have coupled the selectivity associated with the molecular recognition and the sensitivity associated with either radio tracer or fluorescent detection. The proximal probe provides a microfabricated sensor which is capable of detecting a single event. Lee has modified the proximal probe approach into a more robust sensing technology which has already demonstrated an order of magnitude more sensitivity than the present technologies.

1. A. A. Baski, S.C. Erwin and L.J. Whitman, submitted to Surface Science.
2. "Deuterium Processing Stabilizes Silicon Semiconductor Devices," Chemical and Engineering News, March 18. 1996, page 25.
3. S. C. Minne, S. R. Manalis, A. Atalar and C. F. Quate, JVSTB14, 2456 (1996).
4. G.U. Lee, L.A. Chrisey and R.J. Colton, Science 266, 771 (1994); "Getting Physical with DNA," Science News 151, 256 (1997).
5. D.R. Baselt, G.U. Lee, K.M. Hansen, L.A. Chrisey, and R.J. Colton, Proceedings of the IEEE 85, 672 (1997).

Division